

FIG.1A

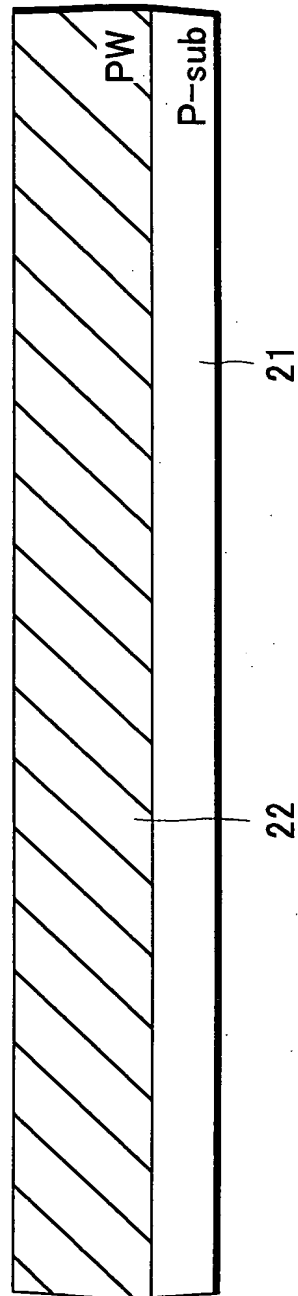
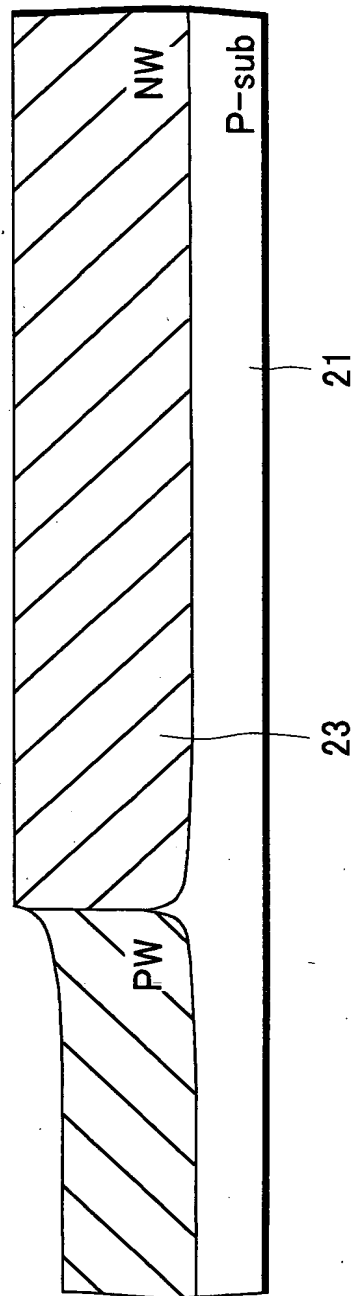
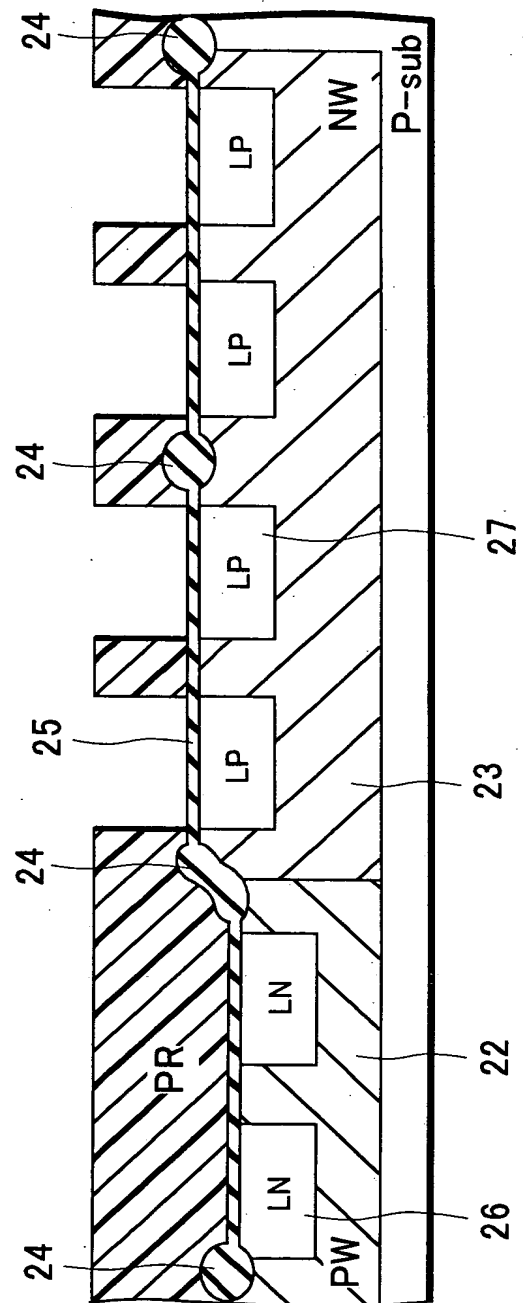


FIG.1B



**FIG. 2B**



This diagram shows a cross-sectional view of a semiconductor device. A central vertical line represents a junction, with circular regions labeled 'PR' (passivation layer) on either side. The device is built on a 'P-sub' (P-type substrate). The top layer is labeled 'PW' (passivation layer). The bottom layer is labeled 'LN' (low-noise layer). The device is divided into sections labeled 24, 25, and 26. The overall structure is labeled 21.

This cross-sectional diagram illustrates a semiconductor device structure. A central channel region, labeled 25, is defined by a series of vertical boundaries. This channel is flanked by regions labeled 24, which contain a material labeled LP. The entire structure is built upon a P-substrate, indicated by the label P-sub at the bottom. On the left side, a region labeled PR is shown, which is adjacent to a layer labeled LN. This LN layer is part of a stack that includes a layer labeled PW. On the right side, a region labeled NW is shown, which is adjacent to a layer labeled LN. This LN layer is part of a stack that includes a layer labeled PW. The top surface of the device is labeled 26, and the bottom surface is labeled 27. The side surfaces are labeled 28 and 29. The device is shown in a cross-section, with the central channel region 25 being the primary feature.

FIG.4A

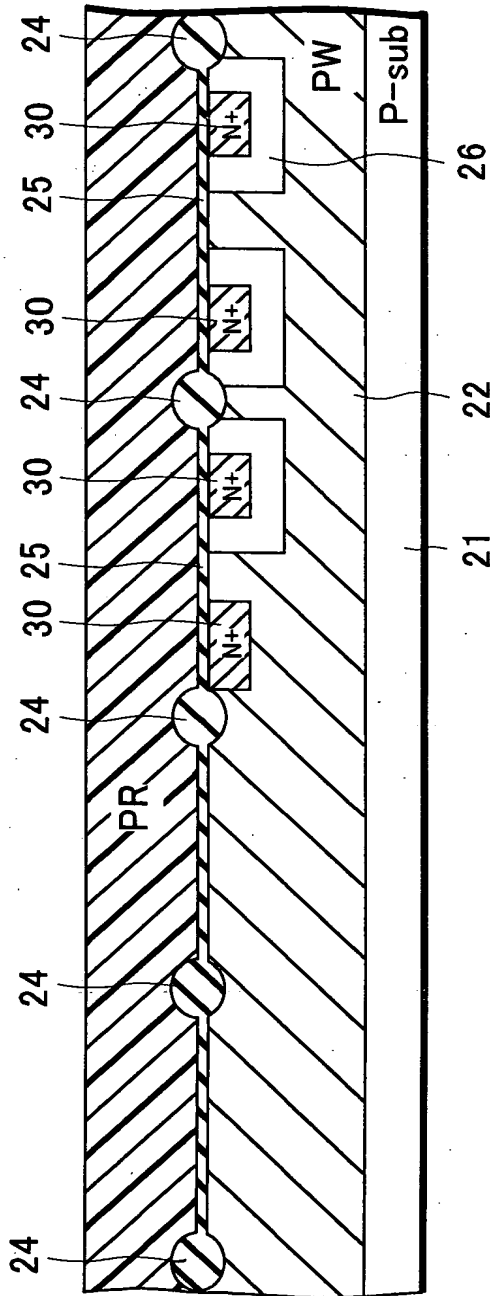


FIG.4B

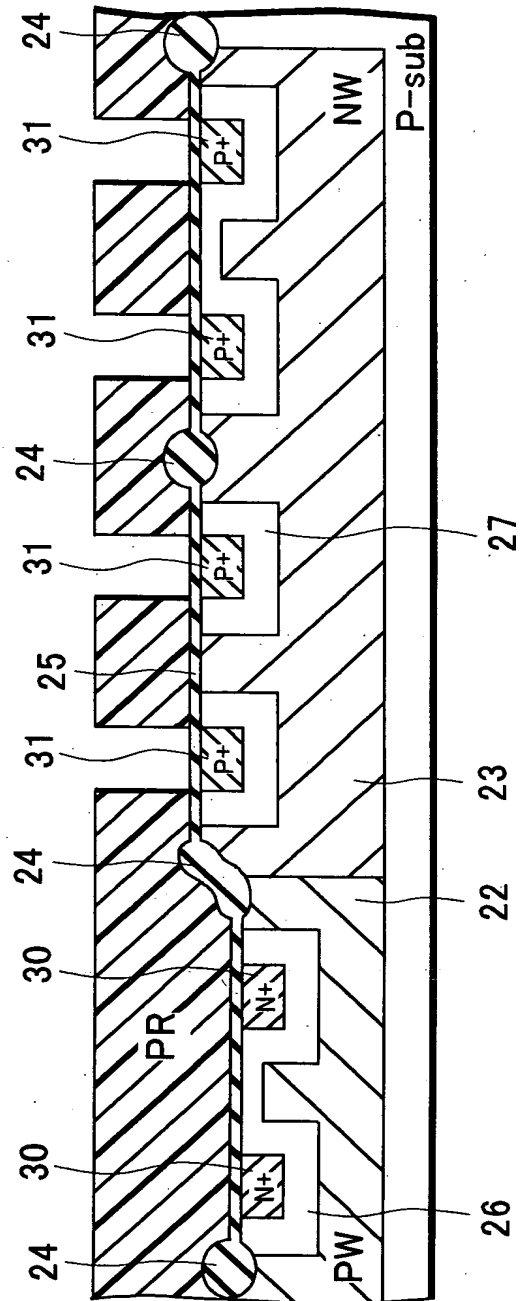


FIG.5A

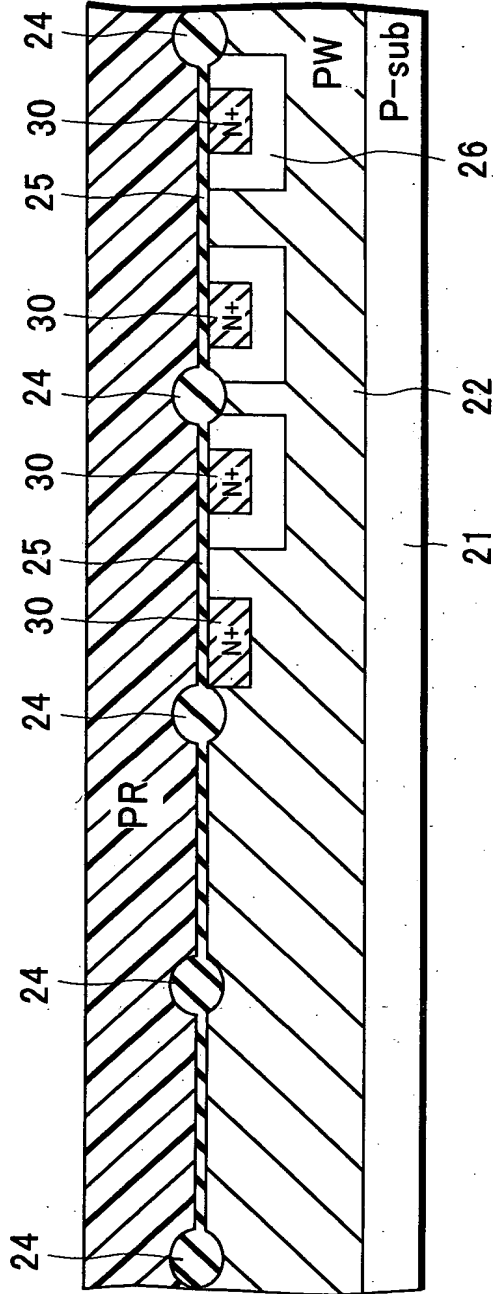


FIG.5B

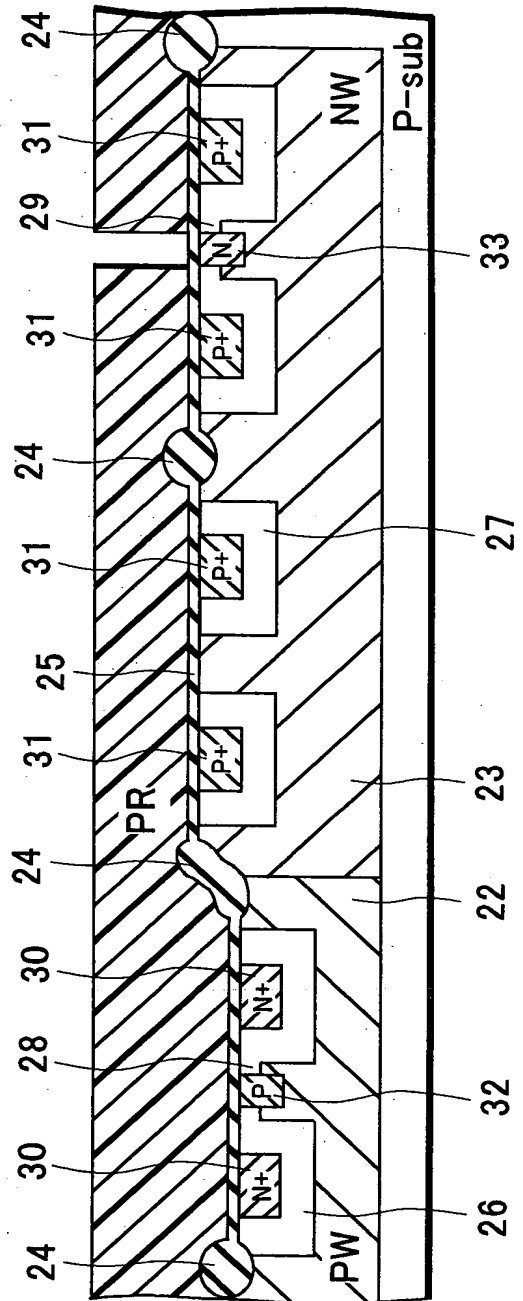


FIG.6A

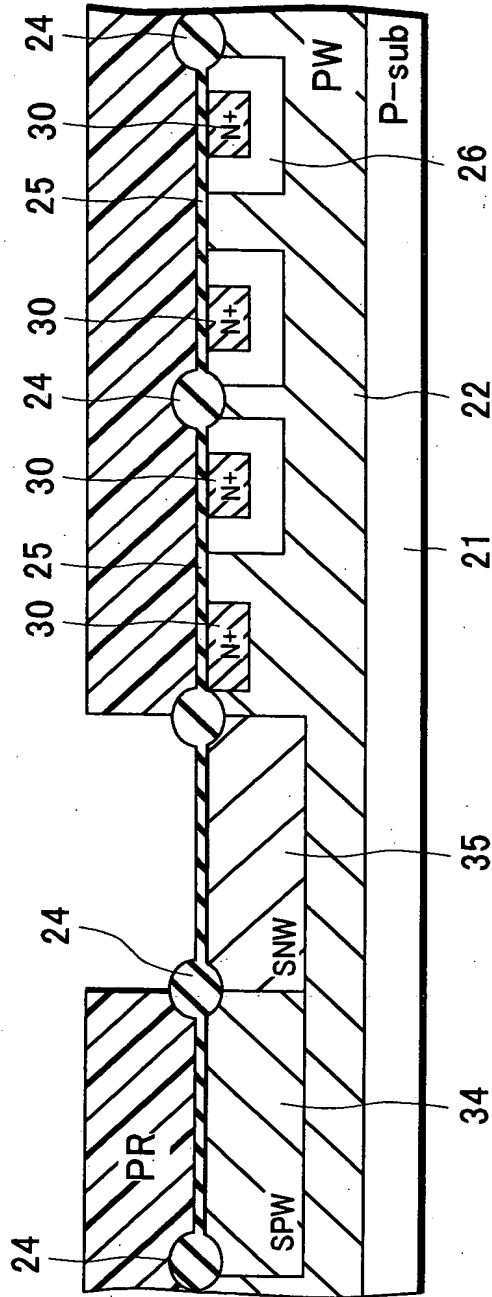


FIG.6B

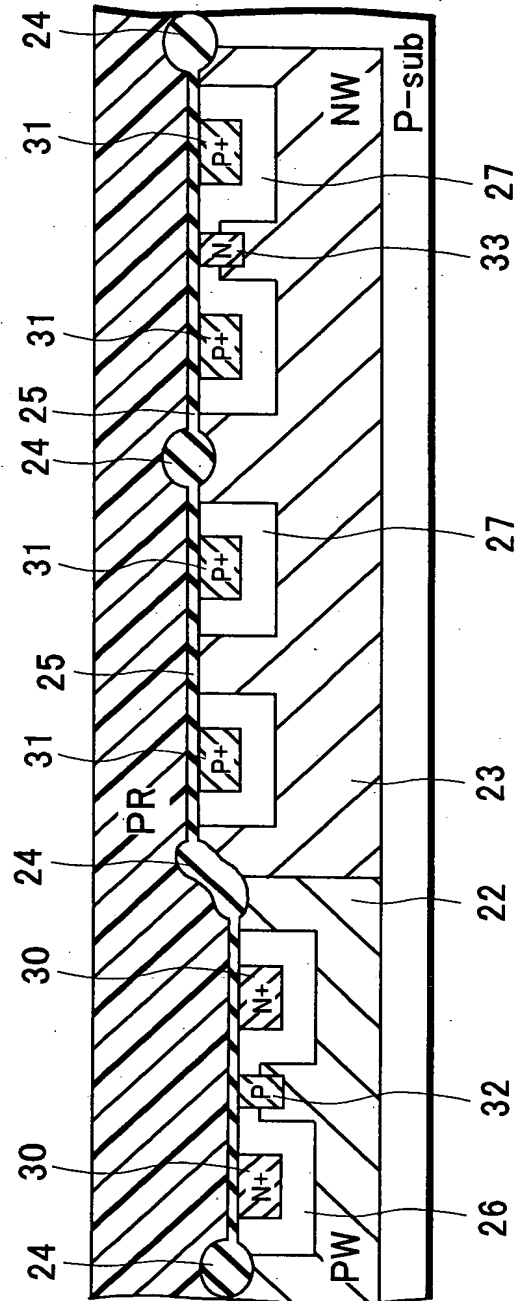


FIG. 7A

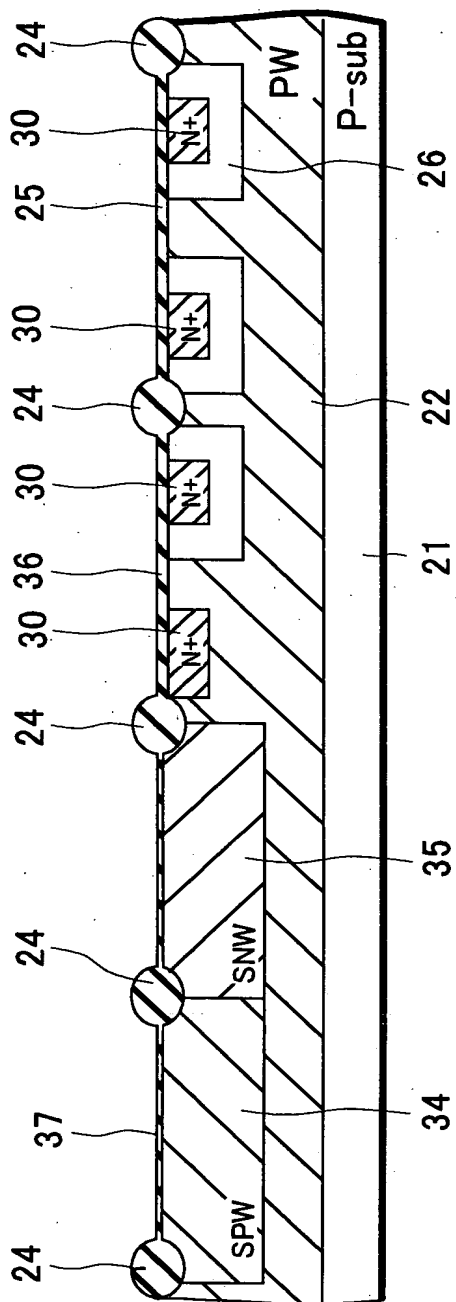


FIG. 7B

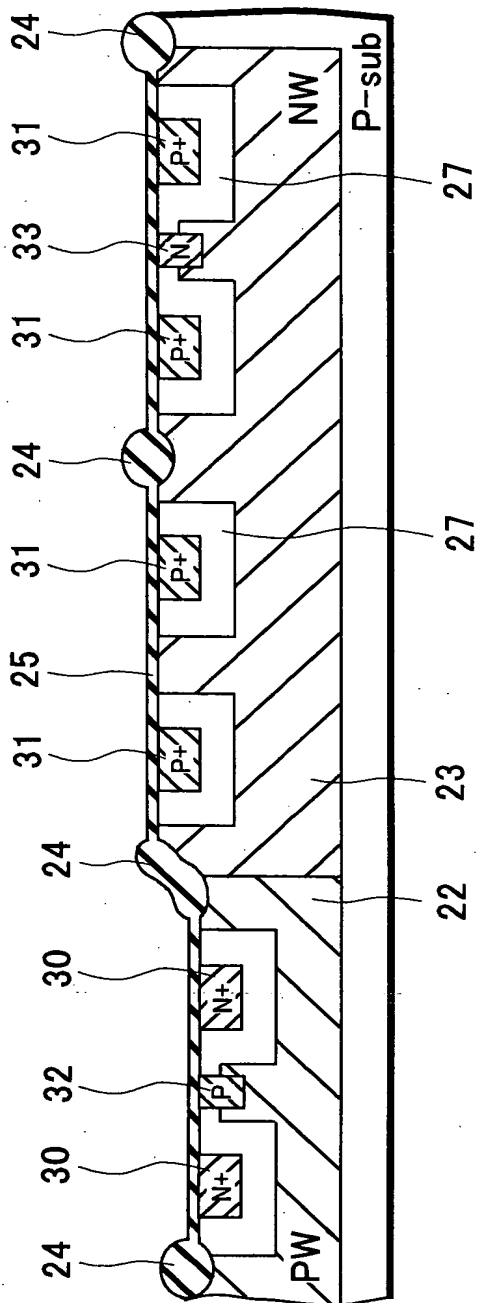


FIG. 8A

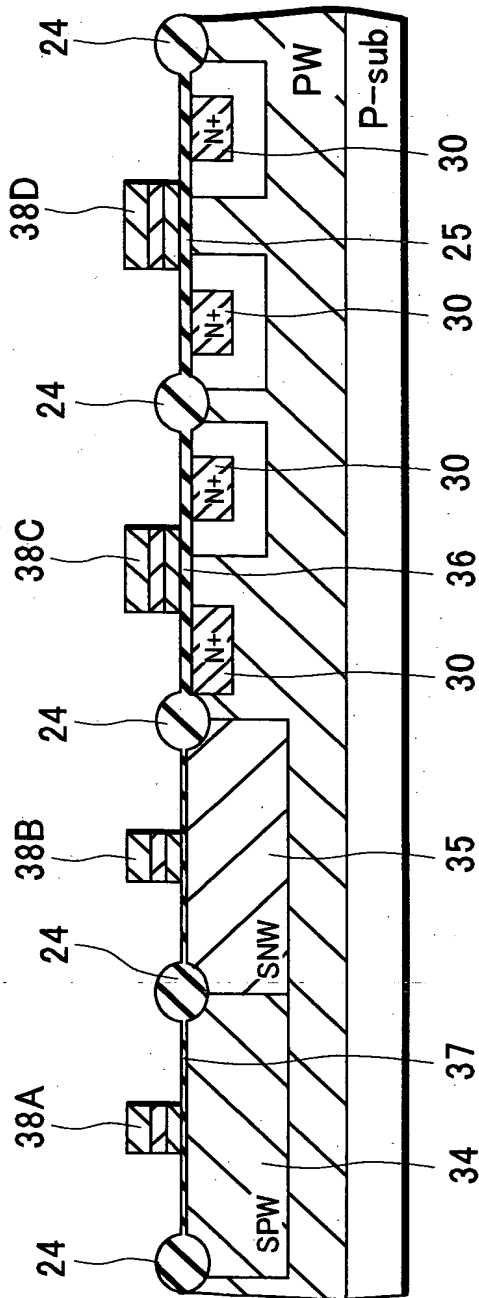


FIG. 8B

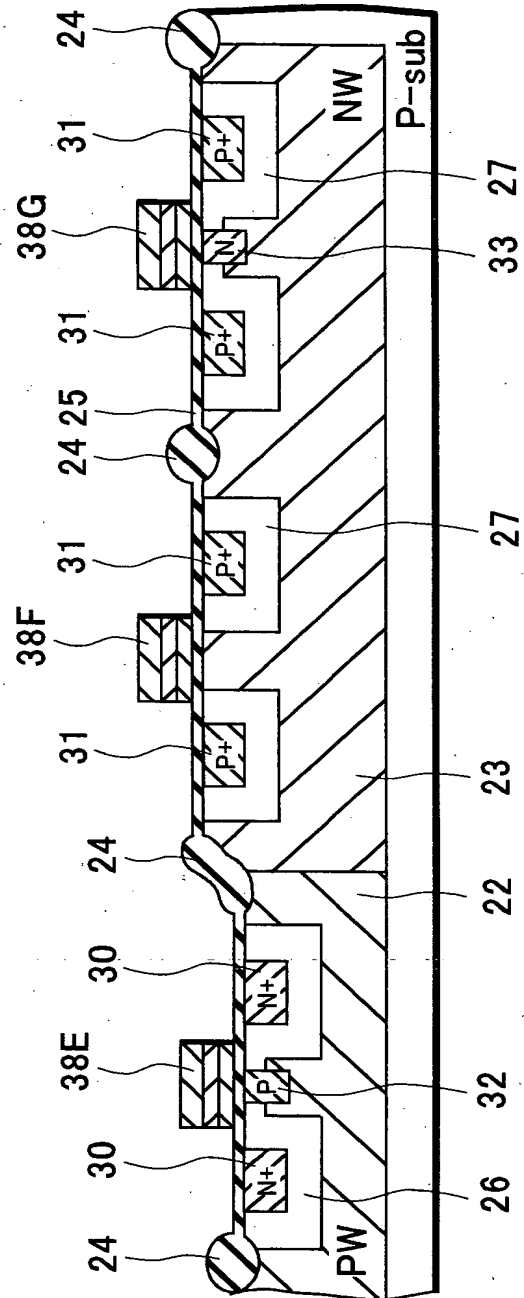




FIG.9A

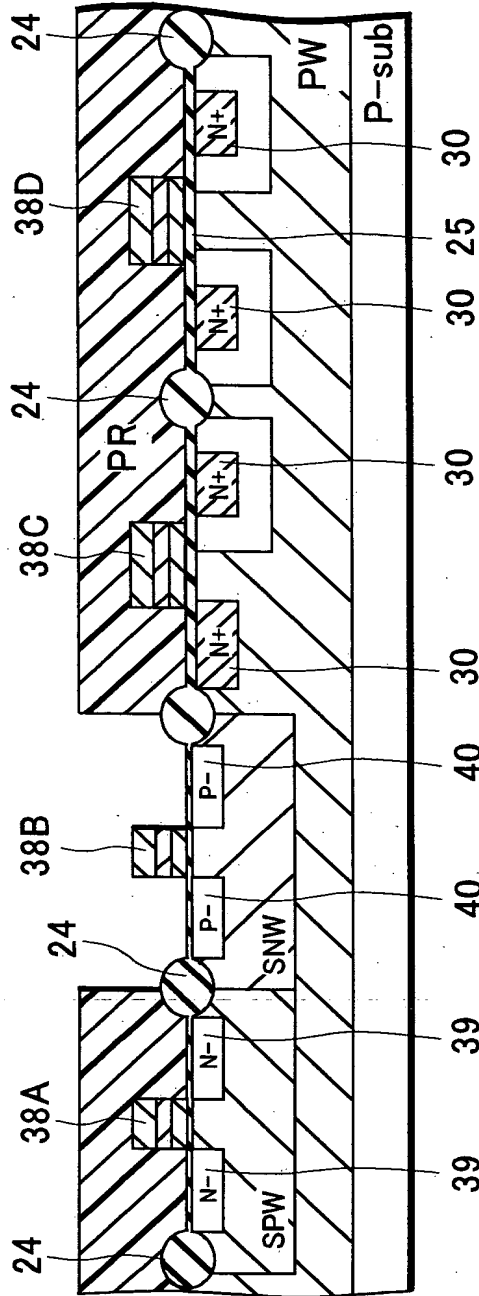
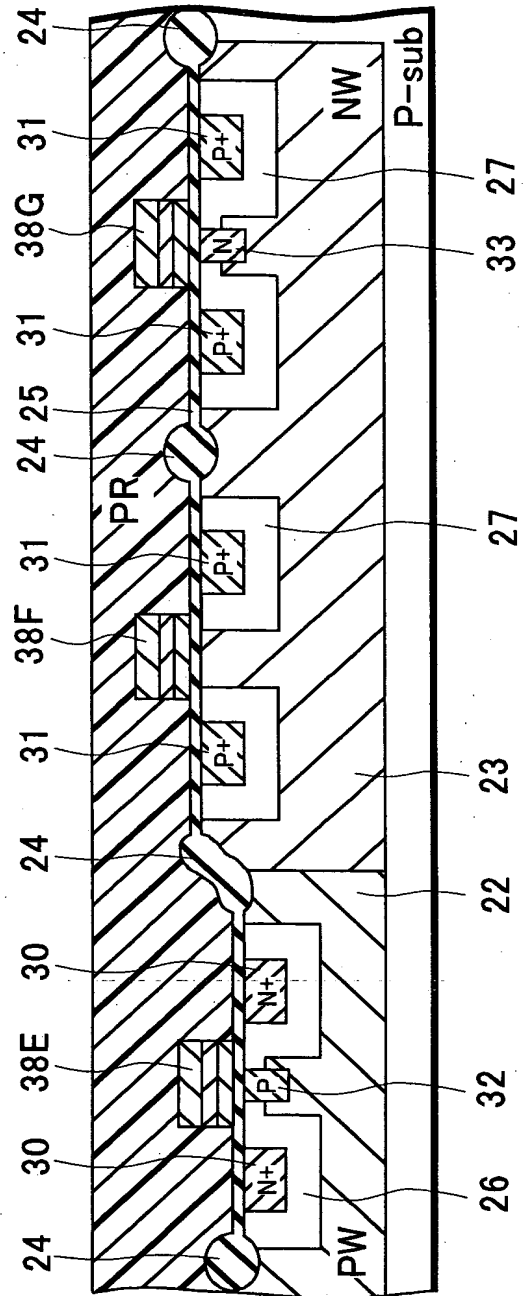


FIG.9B



[illegible]

This diagram shows a cross-sectional view of a semiconductor device. A central channel, labeled 27, is formed in a substrate, labeled 26. The channel is defined by a series of gates, labeled 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, and 41. The gates are formed by a sequence of alternating N+ and P+ regions. The N+ regions are labeled 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, and 41. The P+ regions are labeled 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, and 41. The substrate is labeled 26. The device is shown in a cross-sectional view, with the channel 27 running horizontally. The gates 22-41 are stacked vertically along the channel. The N+ and P+ regions are shown as alternating blocks within the gates. The substrate 26 is the base layer. The labels 22, 23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, and 41 are placed along the top and bottom edges of the diagram, corresponding to the various regions and gates.

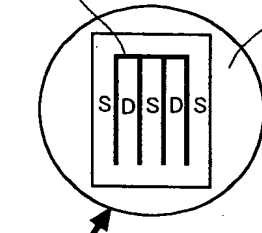
[illegible]

Fig. 1 is a schematic diagram of a semiconductor device. It shows a circular substrate (1) with a rectangular region (2D) containing two vertical lines (SD).

FIG. 12

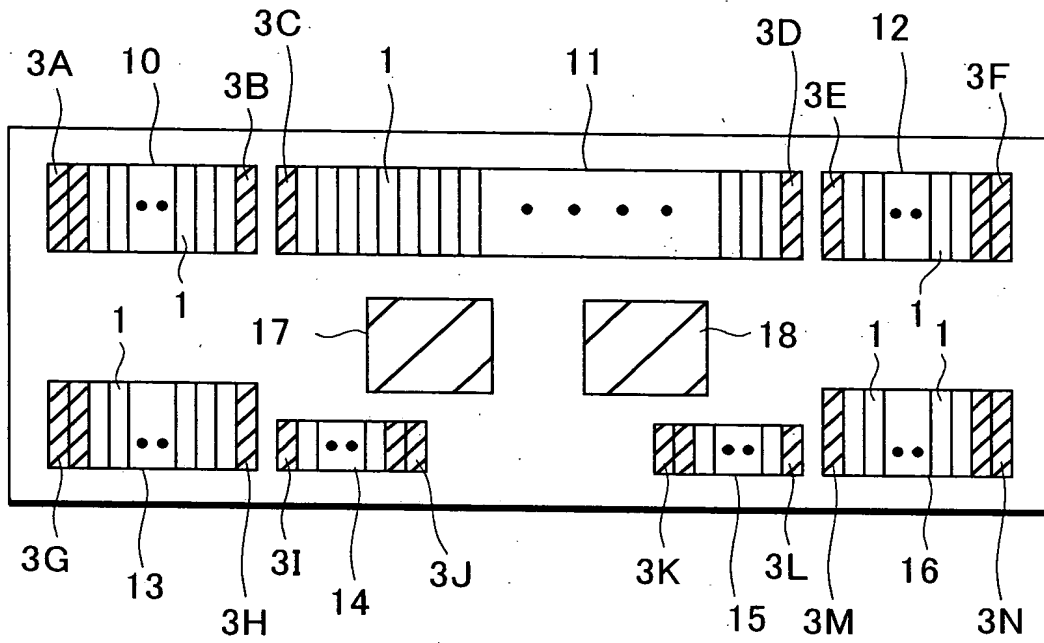


FIG. 13

